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10CS33

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Logic Design

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

PART – A

- 1 a. Define the following : i) Logic Gate and Logic Circuit ii) Fall time and Rise time
iii) Period and frequency iv) Duty cycle [Symmetrical and Asymmetrical]. (08 Marks)
b. What are Universal gates? Prove their universalities. (06 Marks)
c. What is Positive Logic, Negative Logic and Assertion Level Logic? (06 Marks)
- 2 a. A digital system is to be designed in which the days of the week is given as input in 3-bit form. The day Sunday is represented as '000', Monday as '001' and so on. The output of the system has alternate 1's and 0's [ones and zero's] corresponding to the days of the week. Consider the excess number in beyond '110' as don't care conditions. For this system of three variables F(A, B, C) find the following :
i) Truth Table ii) Plot K – map iii) Simplified form of sum of product expression
iv) Simplified form of product of sum expression. (08 Marks)
b. Using Quine Mc – Cluskey method, find the simplified sum of product expression for $F(A, B, C, D) = Y = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$. (10 Marks)
c. Explain Static – 1 hazard. (02 Marks)
- 3 a. What is a Multiplexer? Explain 4:1 MUX with a neat block diagram, functional truth table and an equation. (08 Marks)
b. Implement the function $F(A, B, C, D) = \sum m(0, 3, 4, 7, 8, 10, 11, 13, 14, 15)$ using 8:1 multiplexer. (06 Marks)
c. Realize a full adder using a 3:8 decoder. (06 Marks)
- 4 a. With a neat sketch, explain Master – Slave JK flip flop. (10 Marks)
b. Define the following : i) Flip flop ii) Hold time iii) Propagation delay iv) Set up time v) Characteristic equation. (10 Marks)

PART – B

- 5 a. Draw the logic diagram of a 4-bit serial in serial out shift register using D – flip flop. Show the appropriate waveform and state table for shifting – in the input '0010'. (10 Marks)
b. List the applications of shift register. Explain Sequence Generator and Sequence detector. (08 Marks)
c. How long will it take to shift an 8-bit number into a 54164 shift register if the clock is set at 10 MHz? (02 Marks)
- 6 a. With a neat logic diagram, truth table and waveform, explain a 3 – bit binary ripple up – counter (Asynchronous). (10 Marks)
b. Design a synchronous Mod – 5 counter. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.



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- 7 a. Write short notes on :
- i) Mealy model ii) Moore model. (10 Marks)
- b. What is an Algorithmic State Machine? What are the advantages of using ASM chart? Draw an ASM chart following Mealy model for the vending machine problem. (10 Marks)
- 8 a. Define a Binary ladder and draw a binary ladder for 4-bits. Design and explain a binary ladder with a digital input of '1000' and construct an equivalent circuit for the same. (10 Marks)
- b. Define the following :
- i) Binary Equivalent Weight.
 - ii) Millman's theorem.
 - iii) Analog to Digital conversion.
 - iv) Digital to Analog conversion. (10 Marks)
